ALSETlab

Submission #8

MMChvdcLibrary: Modeling Arm Average Value Modular Multilevel Converters in Modelica for Power System Simulation

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RPI

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https://alsetlab.github.io/

Library on GitHub
(BSD 3-Clause)

Why Phasor-Domain MMC Models?

MMC is the workhorse of HVDC

- Higher power-handling capability.
- Less switching power losses and harmonic distortion.
- Reference topology for modern HVDC links and future MTDC grids.

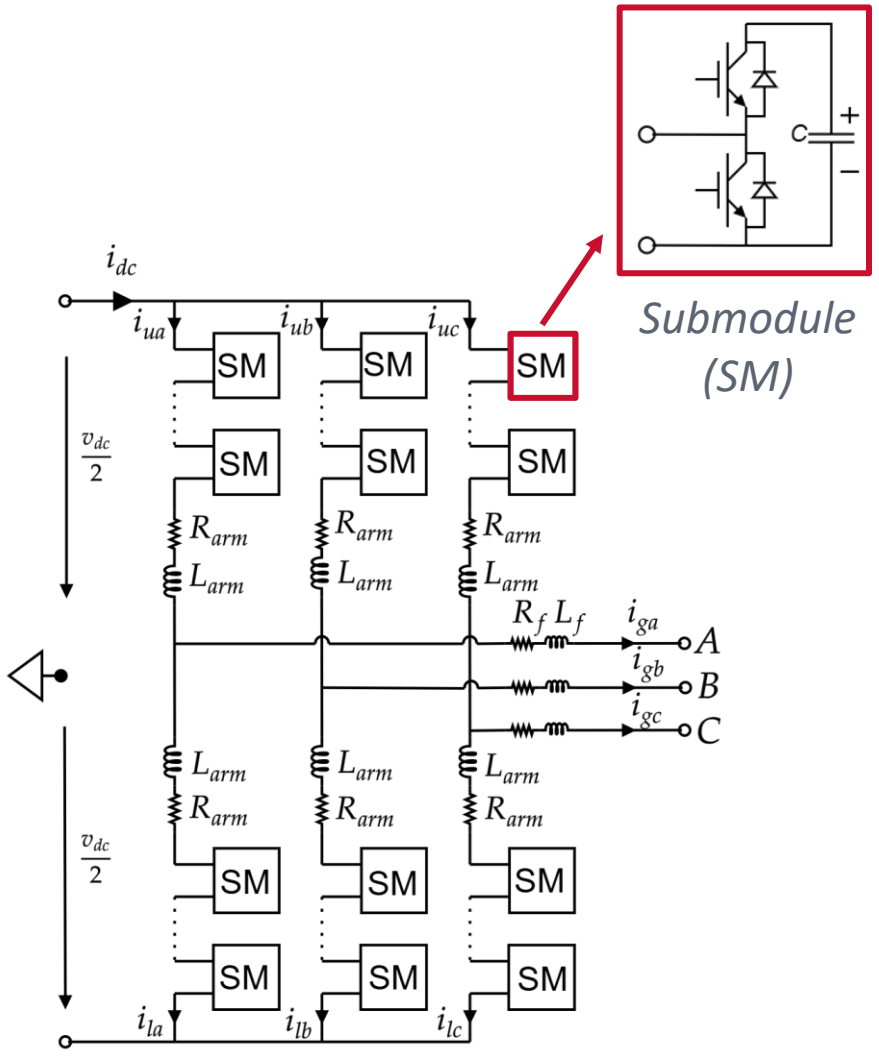
EMT models

- Reproduce switching-level phenomena accurately
- EMT models are computationally heavy for large grids.
- Poorly suited to system-wide transient stability studies

Phasor-domain arm average value models

- Keep the essential average dynamics of the EMT models, including internal stored energy
- Fast enough for large-scale system simulation
- Interface directly with phasor-domain AC network libraries (OpenIPSL)

Gap: no structured, multi-control mode, openly available MMC-HVDC Modelica library exists.



Detailed three-phase MMC circuit.

MMChvdcLibrary at a Glance

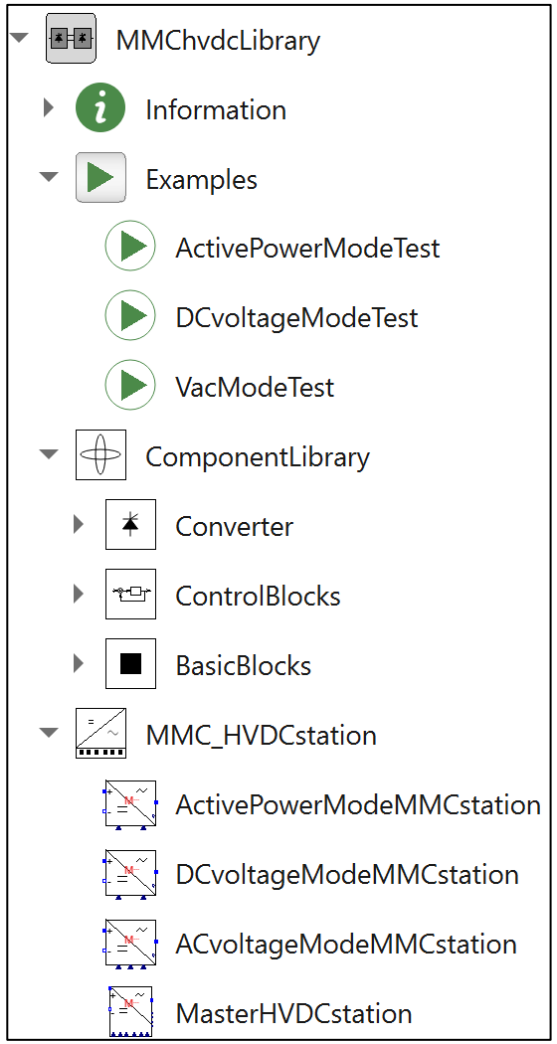
MMChvdcLibrary

- A Modelica library developed in Dymola.
- For phasor-domain arm average value modeling of MMC-HVDC systems.
- Designed for seamless integration with OpenIPSL to couple with the AC network.

Package structure of the MMChvdcLibrary

- **Information:** model, control, and usage documentation.
- **Examples:** one test model per operating mode
- **ComponentLibrary**
  - Converter: phasor-domain AAVM MMC model
  - ControlBlocks: outer- and inner-loop controllers, synchronization
  - BasicBlocks: dq transforms, sensors, power and energy calculators, PLL
- **MMC_HVDCstation:** four ready-to-use station models
  - ActivePowerModeMMCstation: *P-Q* control
  - DCvoltageModeMMCstation: *Vdc-Q* control
  - ACvoltageModeMMCstation: *Vac* phasor control
  - MasterHVDCstation: reconfigurable control station integrating all three controls.

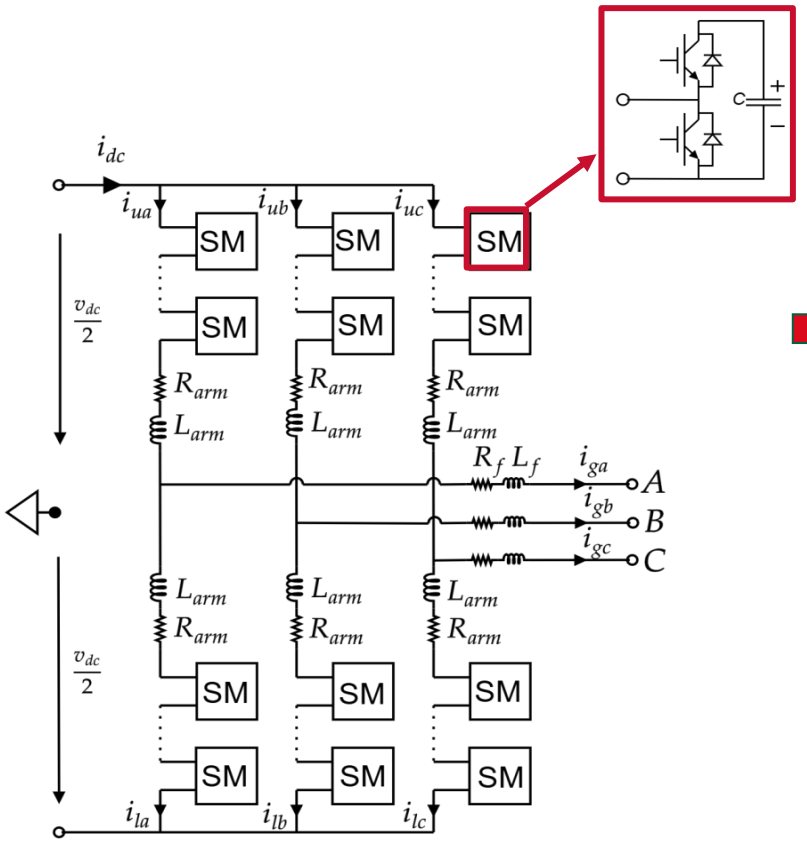
Dependencies: Modelica Standard Library 4.1.0, OpenIPSL 3.1.0



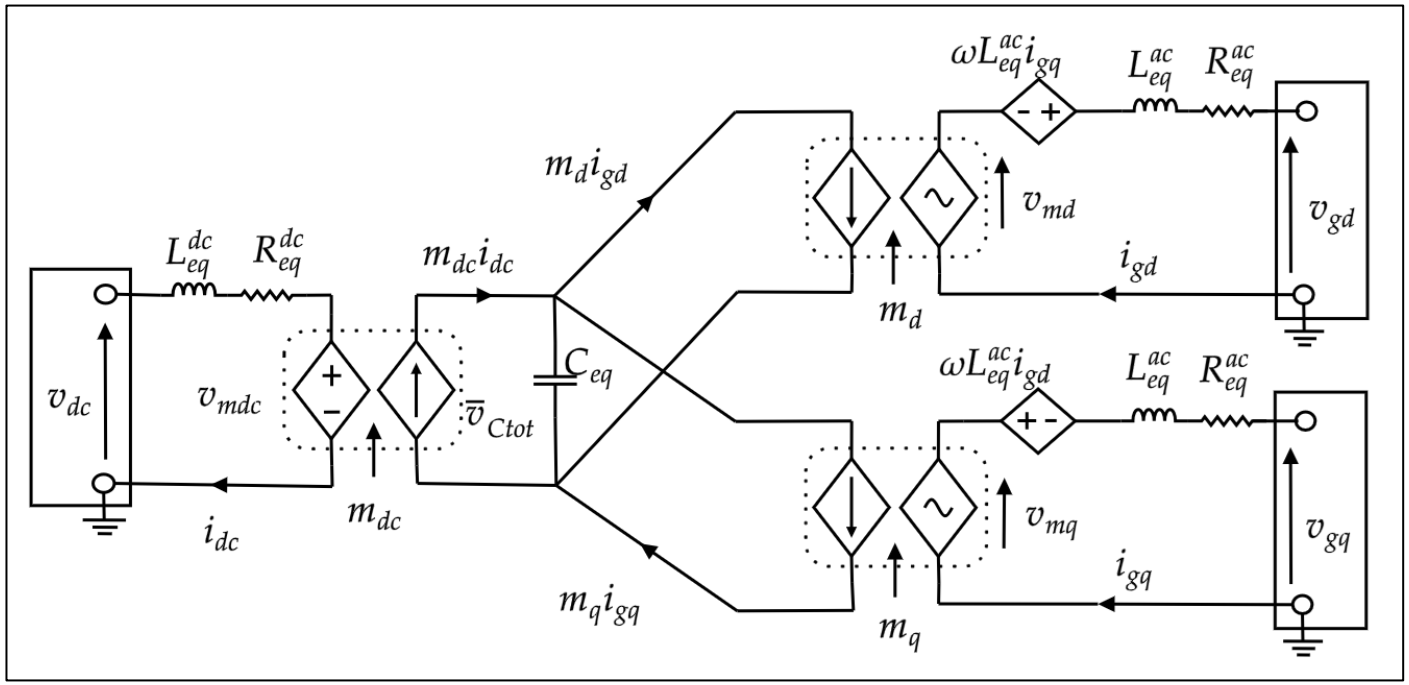
MMChvdcLibrary package structure.

Converter Model: From EMT circuit to Phasor

- The simplified Phasor-domain AAVM model of the MMC captures the converter's internal energy dynamics without modeling individual switching events.
- Modulated voltages v_{md}, v_{mq} and v_{mdc} are the control inputs.



Detailed three-phase MMC circuit.



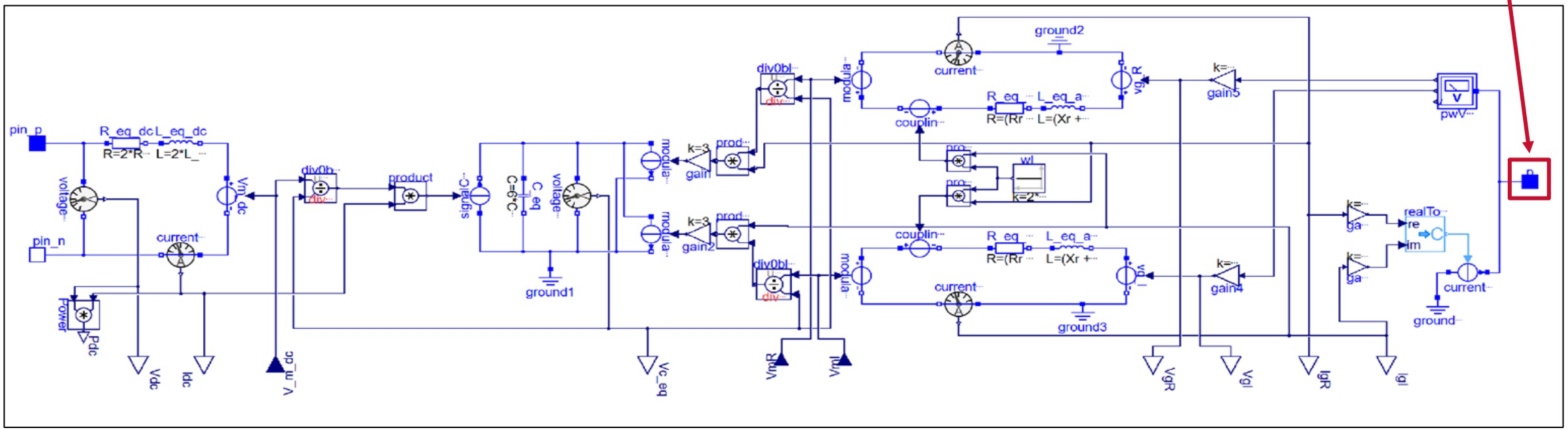
Phasor-domain MMC model.

Key assumptions

- Balanced SM capacitor voltages within each arm.
- Energy shared equally between phases.

Converter Model: Dymola Implementation—AvgMMCmodel

- Electrical circuit and the mathematical operations required by the converter built from the **MSL v4.1.0 .**
- The ***RealToComplex*** block is used to convert real-valued signals into complex variables.
- The **OpenIPSL (v3.1.0) Library** is mainly used to implement the converter AC terminal voltage to the interface with the phasor network.
- Model initialization is performed in the Dymola text layer: the user provides the power-flow data.



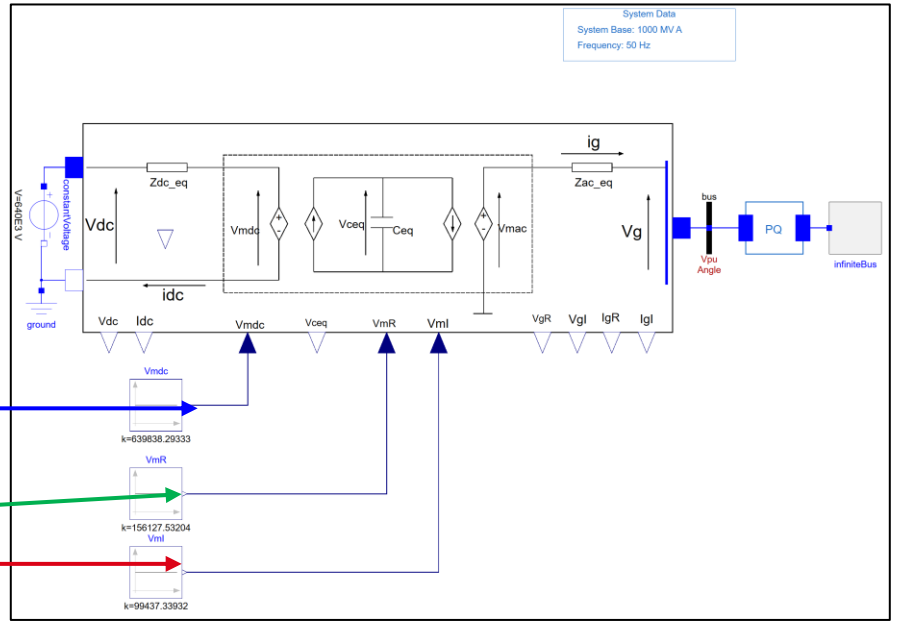
Phasor-domain MMC model implementation in Dymola.

Converter Model: Initialization of the AvgMMCmodel

Steady state analysis to evaluate control inputs : Vmdc, Vmr, & Vmi

```
--- Inputs  ---
Vg (Grid voltage magnitude) = 320000.00000 V
angle_0 (Grid voltage phase angle) = 30.00000 degrees
P_ref (AC Power reference) = 200.00 MW

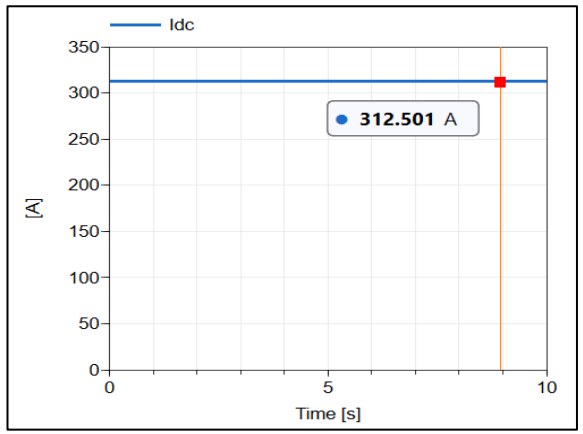
--- Results ---
Idc (DC current) = 312.50000 A
VgR (Real part of grid voltage) = 160000.00000 V
VgI (Imaginary part of grid voltage) = 92376.04 V
IgR (Real part of grid current) = 312.50000 A
IgI (Imaginary part of grid current) = 180.42196 A
VmR (Real part of modulated AC voltage) = 156127.53204 V
VmI (Imaginary part of modulated AC voltage) = 99437.33932 V
Vmdc (Modulated DC voltage) = 639838.29333 V
```



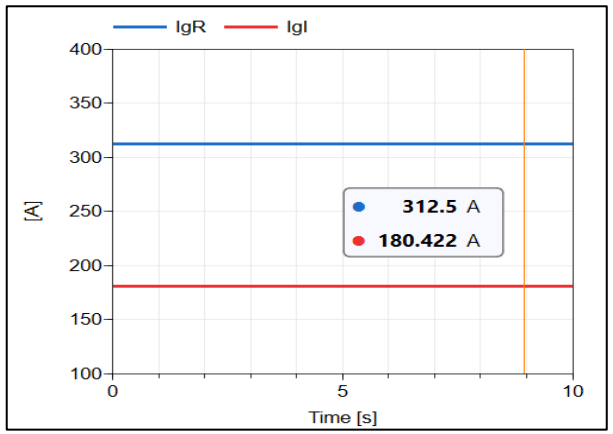
Test system of the MMC model for calculated control inputs

Flat starting point: Proper Initialization

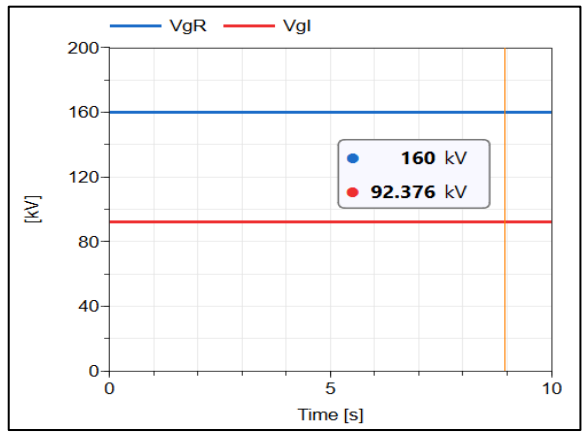
DC Current



AC real and imaginary current

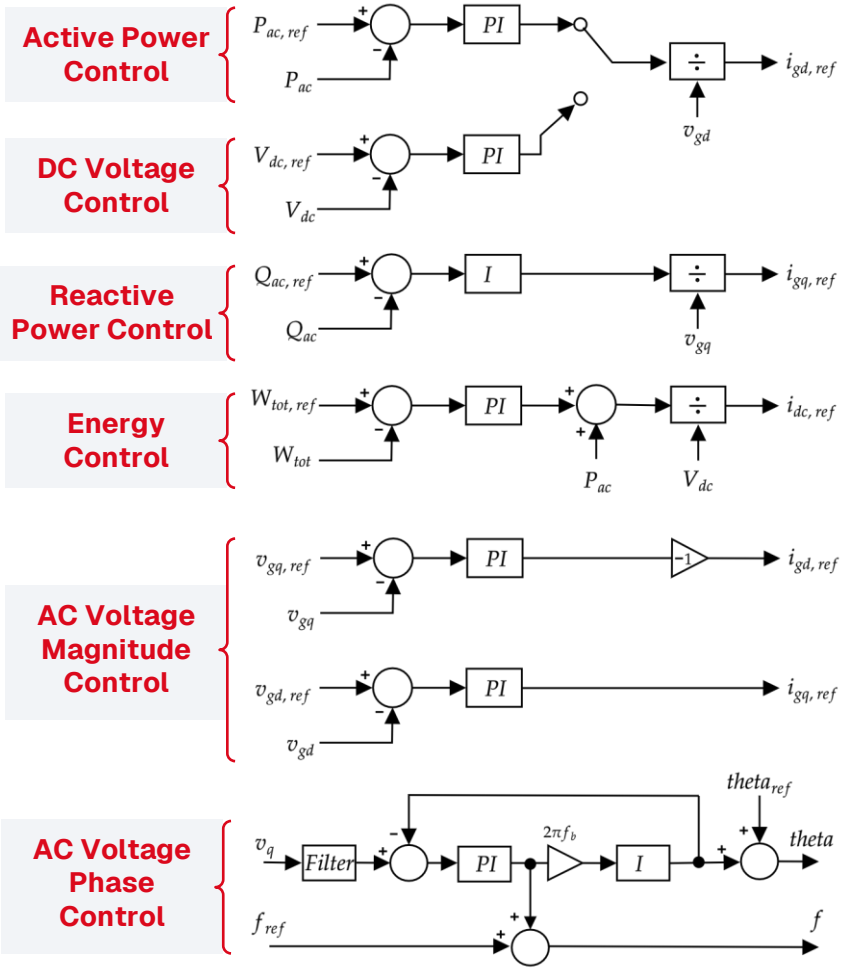


AC real and imaginary voltage

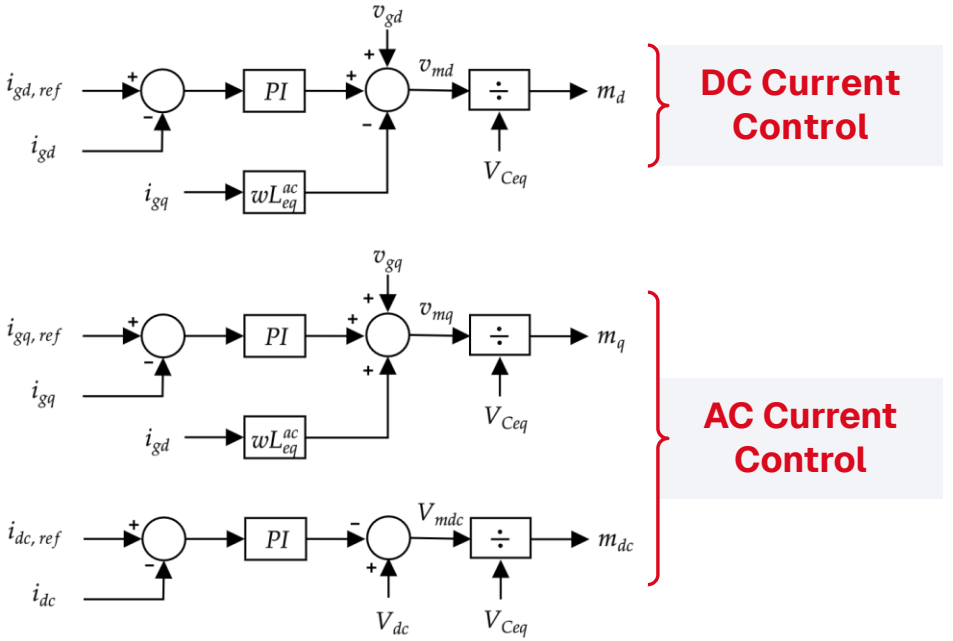


Control Blocks

Outer loops set references, and inner loops track them



Outer-loop controllers.

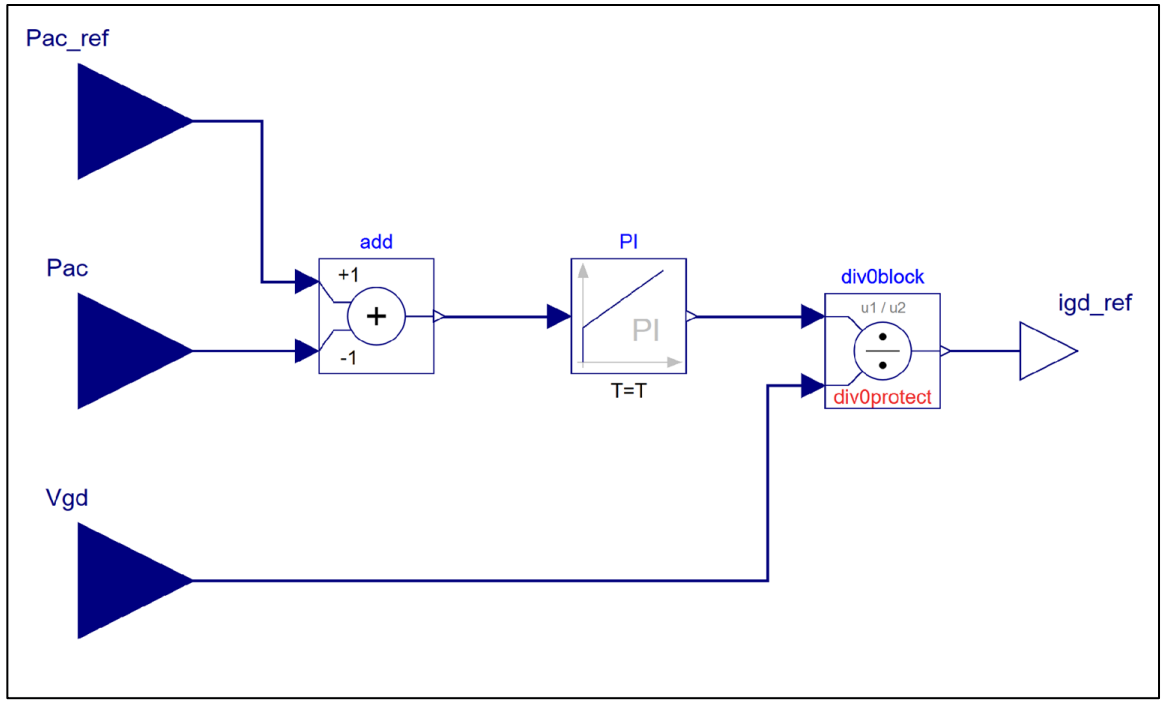


Inner-loop controllers.

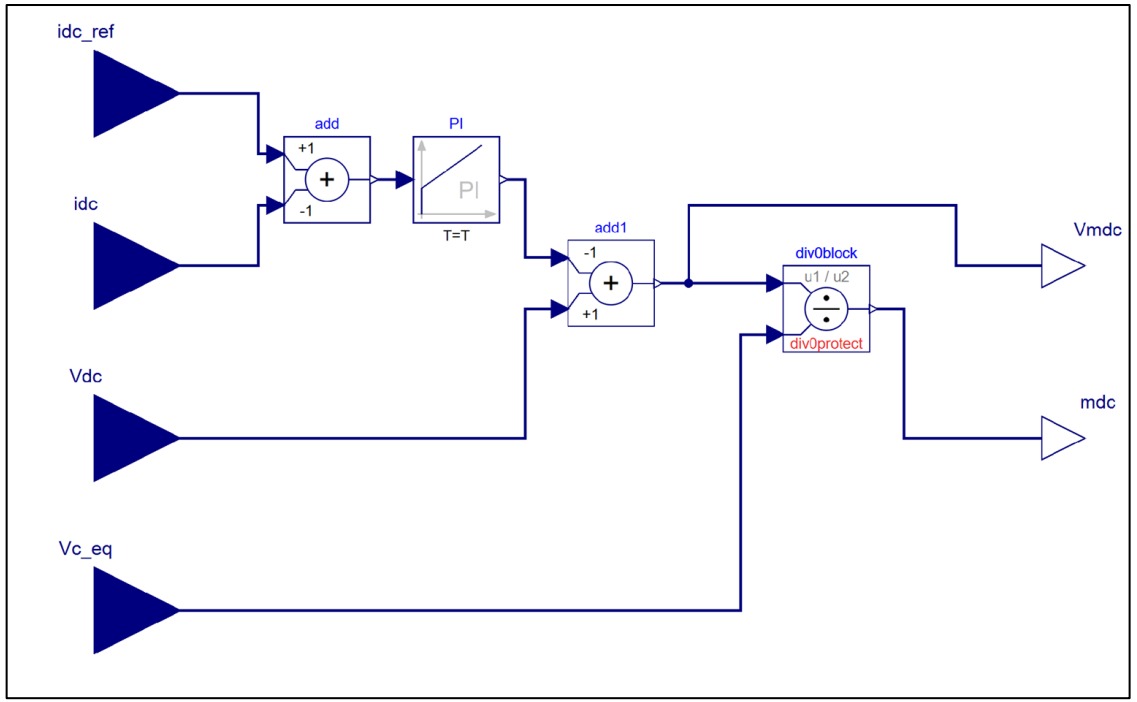
- **Outer loops:** EnergyControl, ActivePower/DCvoltage, and ReactivePower control produce current references.
- **Inner loops:** d/q-axis AC and DC current control, giving the modulation indices *md*, *mq* and *mdc* via V_{Ceq}.

Control Blocks: Dymola Implementation

- The control blocks built graphically from **MSL** and **OpenIPSL** blocks, with divide-by-zero protection
- PI controller gain k and time constant T propagate to the higher-level station model, so the controller can be tuned directly from the station interface.
- All the control blocks in the library are implemented in a similar way.



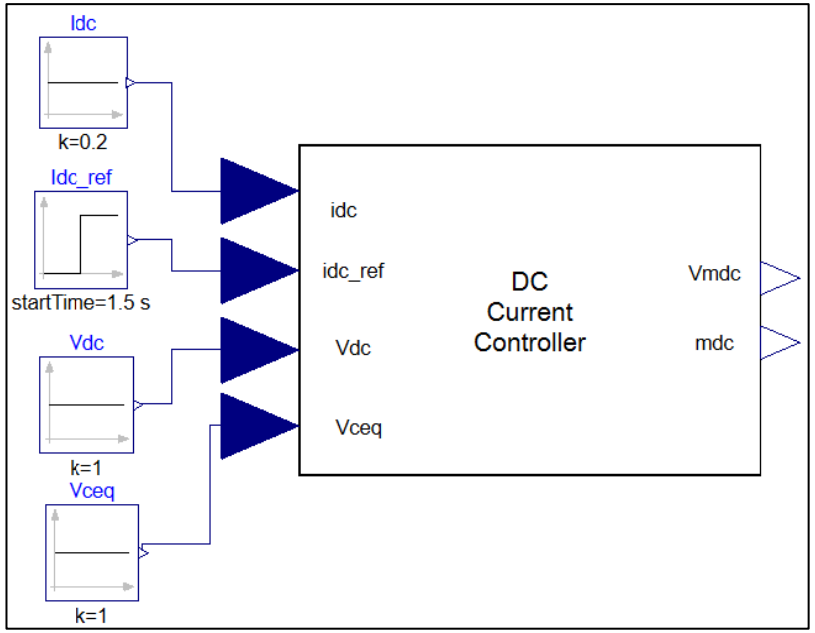
Outer-loop controler: *ActivePowerControl.*



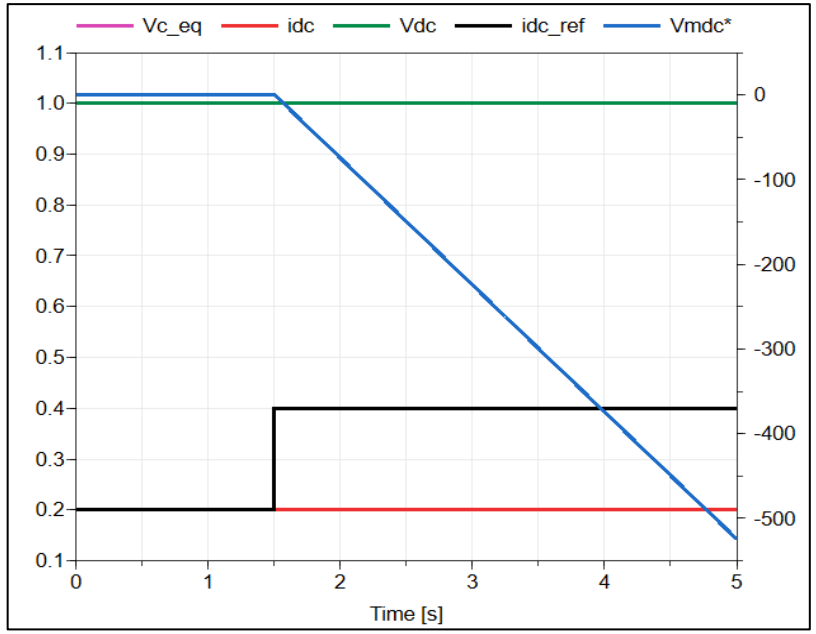
Inner-loop controller: *DCcurrentControl.*

PI control block initialization test

- At t = 1.5 s, the DC current reference **id_ref** increases from 0.2 to 0.4.
- The actual DC current **idc** remains flat at 0.2 (no plant is connected).
- The modulated DC voltage **Vmdc** drops rapidly after 1.5 s due to **integral action**, reaching large negative values.
- The controller is active, producing a sharp voltage command to **drive the current up**.
- The process of initialization for all the control blocks are similar.



DC current Controller test

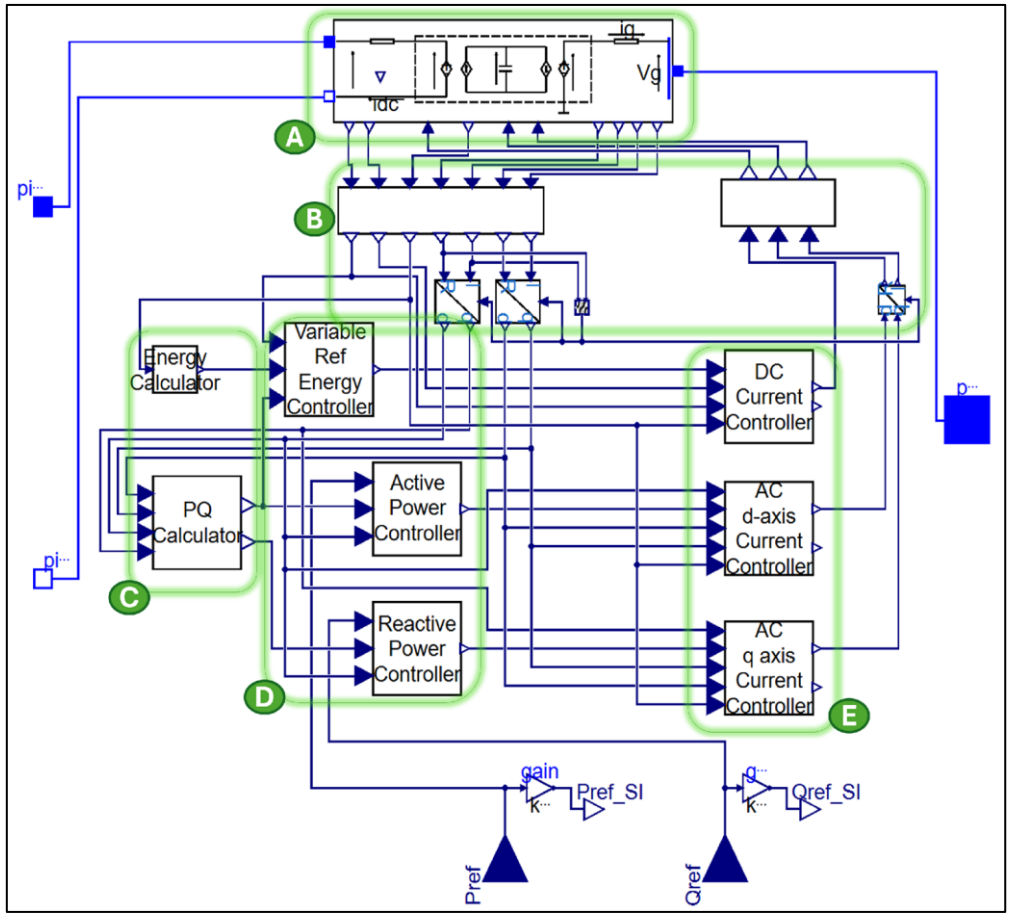


Controller response

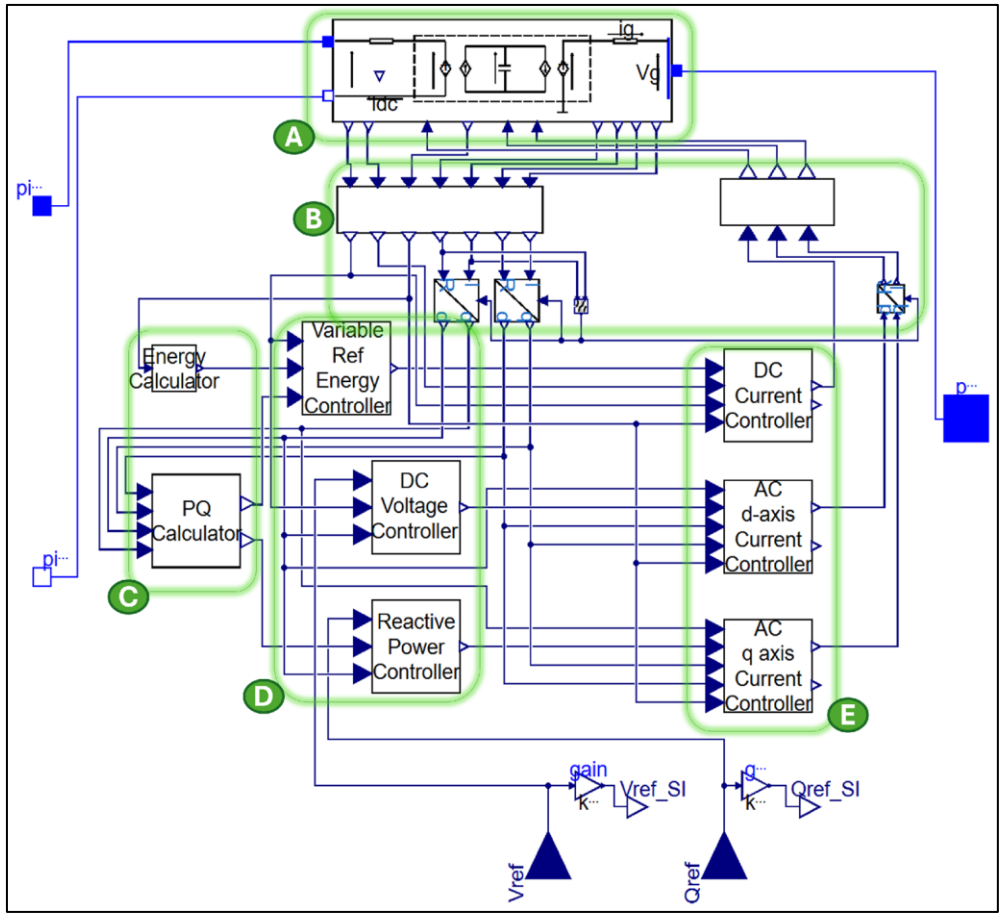
MMC_HVDCstation: P-Q and Vdc-Q Stations

Zones:

- A: converter
- B: transformations
- C: PQ/energy calculators
- D: outer loops
- E: inner loops



ActivePowerModeMMCstation.



DCvoltageModeMMCstation.

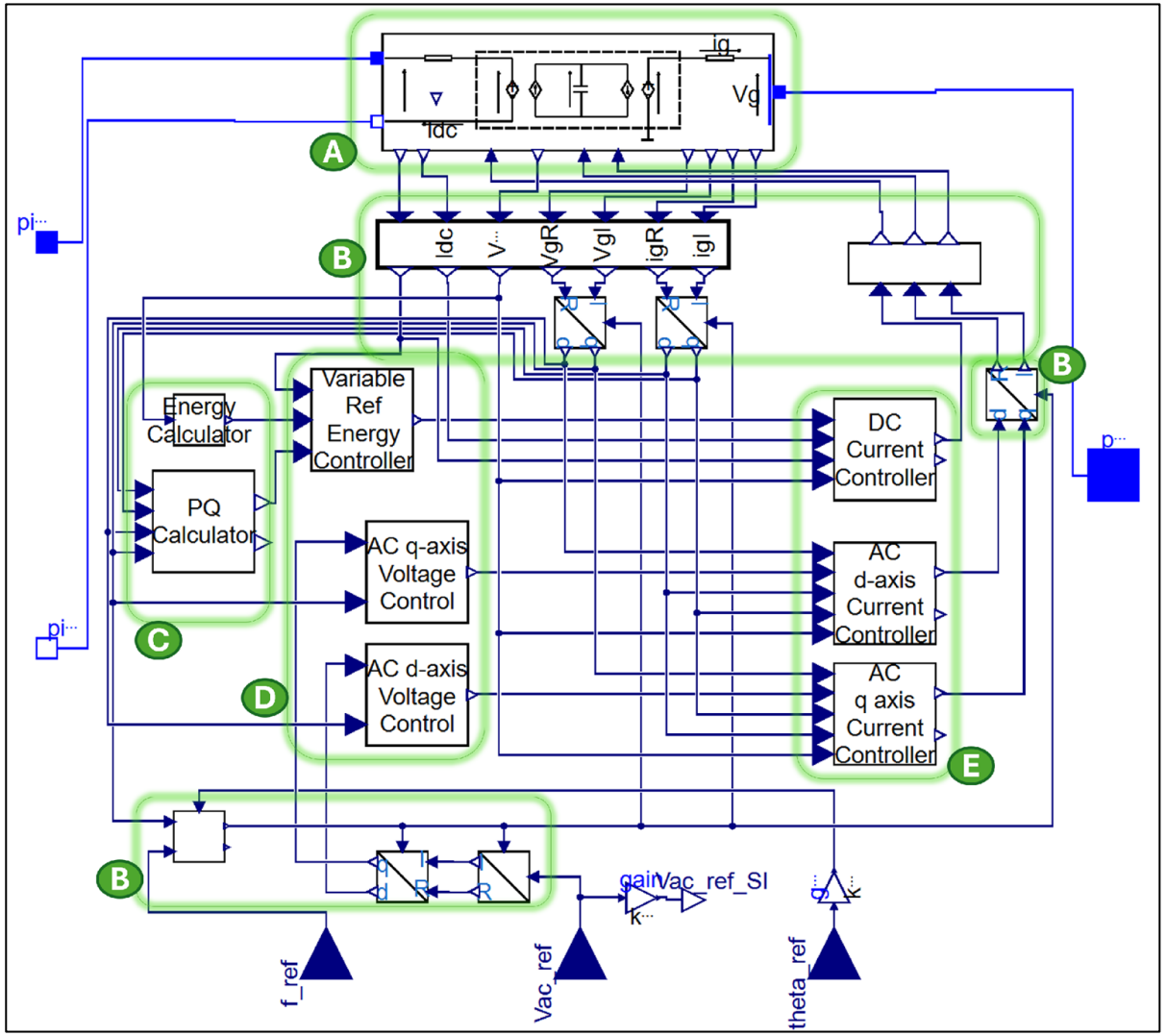
- **Zone D** holds energy, active-power (or DC-voltage), and reactive-power control blocks.
- In the DCvoltageModeMMCstation, the DC Voltage Controller replaces Active Power Controller in **zone D**.

MMC_HVDCstation: Vac Station

- **Zone D:** AC Voltage Controller replaces the power-regulating blocks.
- **Zone B:** A Synchronization block supplies the phase angle (θ) and frequency (f) for all dq transformations.

Zones:

- A: converter
- B: transformations
- C: PQ/energy calculators
- D: outer loops
- E: inner loops



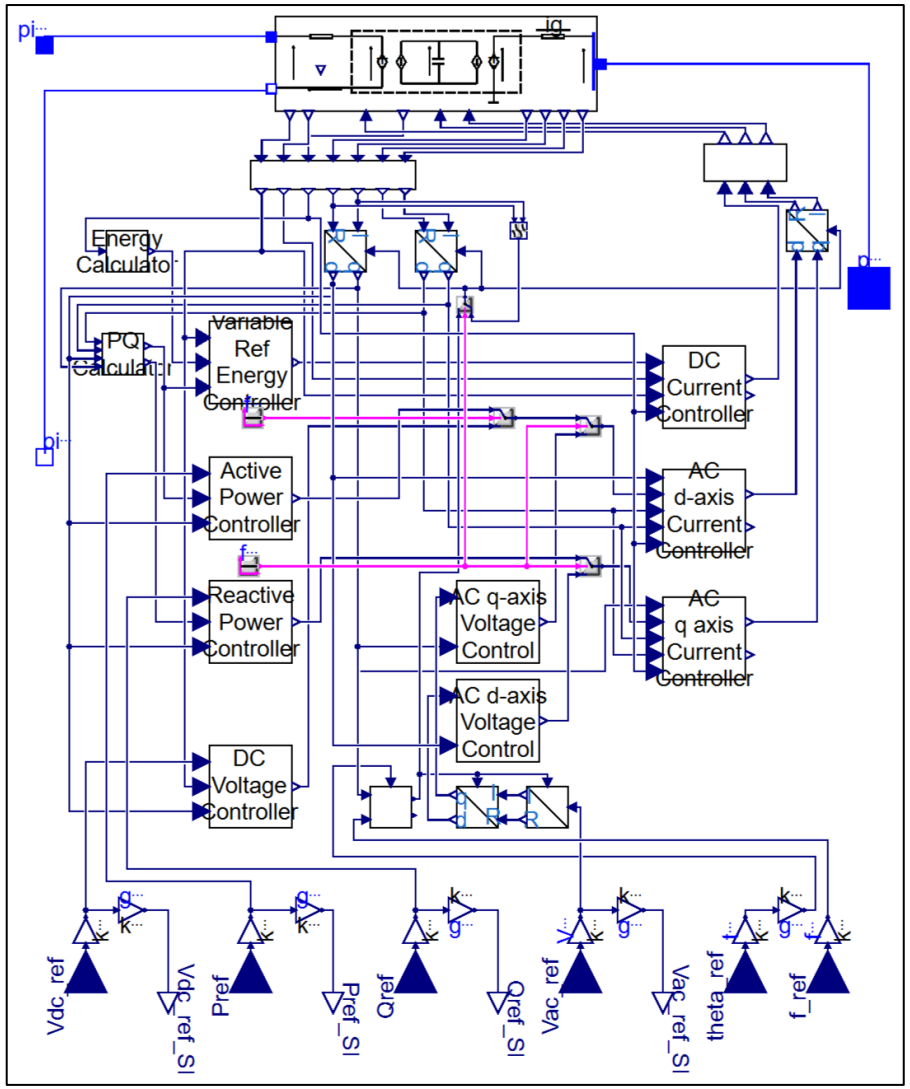
ACvoltageModeMMCstation.

MMC_HVDCstation: MasterHVDCstation

- All three operating modes in a single component
- Two Boolean parameters **(Vdc_Pac_flag** and **Vac_Qac_flag)** select the mode, so the same instance can play any role in an HVDC link.

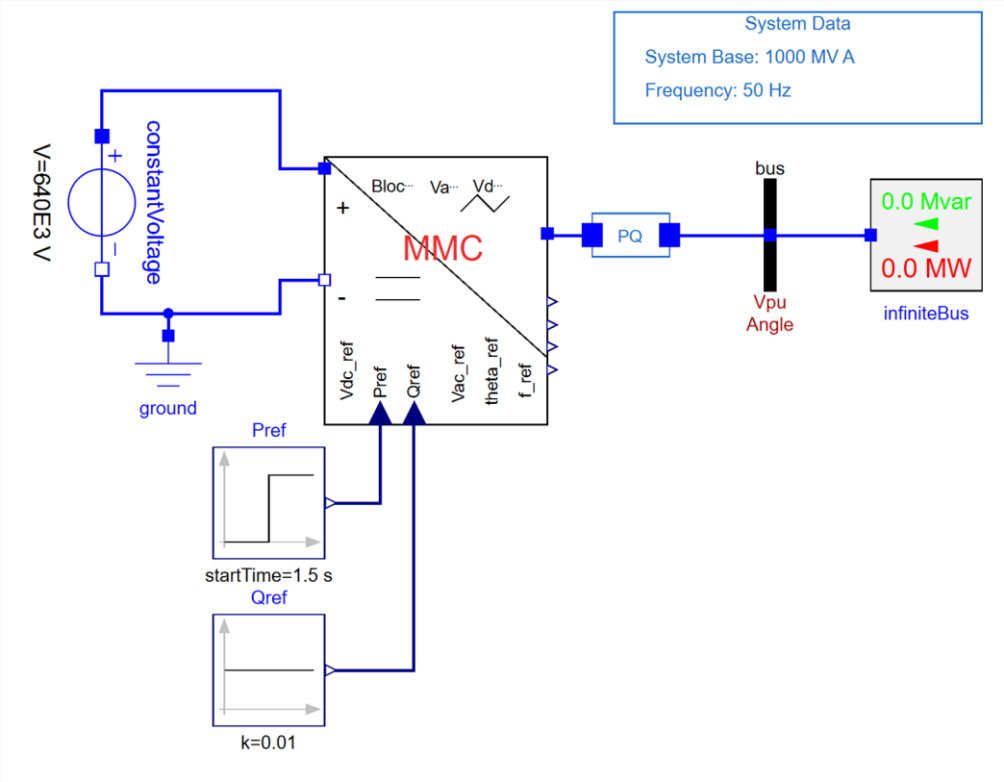
Vdc_Pac_flag	Vac_Qac_flag	Control mode
true	true	Pac-Qac
false	true	Vdc-Qac
true	false	Vac
false	false	No control

Mode-selection logic of the MasterHVDCstation.

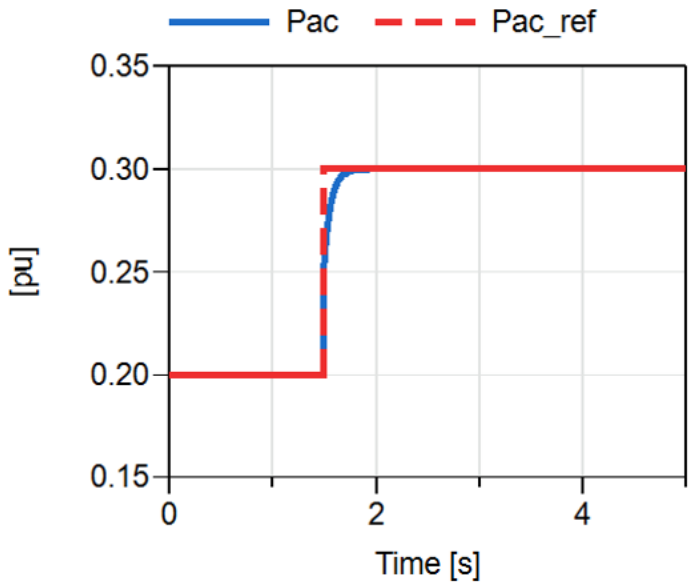


MasterHVDCstation implementation.

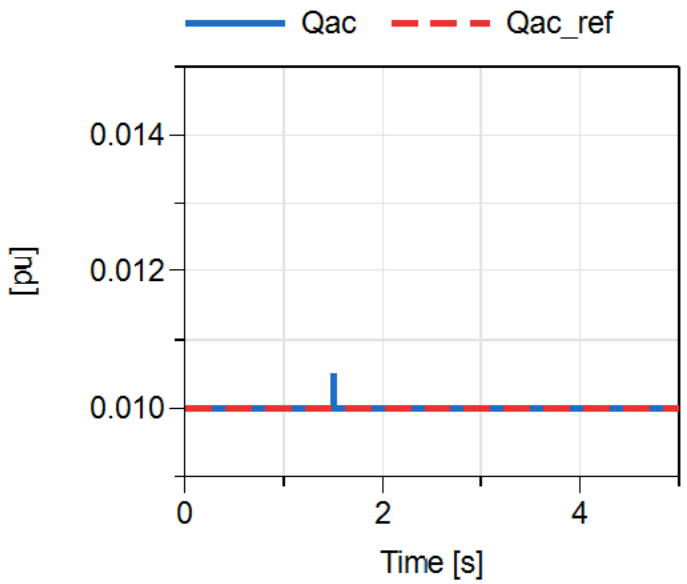
Examples: Active Power Mode Test



ActivePowerModeTest model



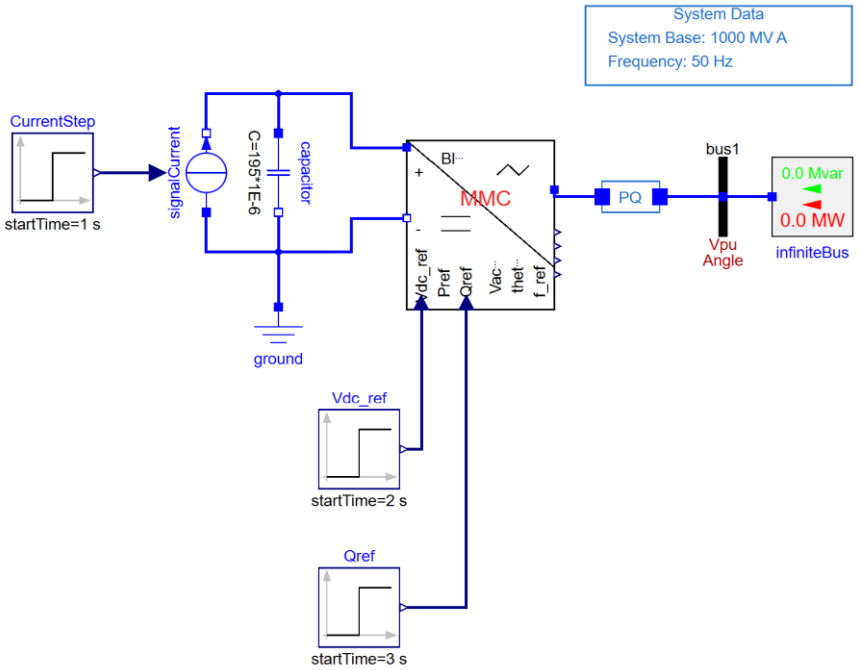
Pac response;



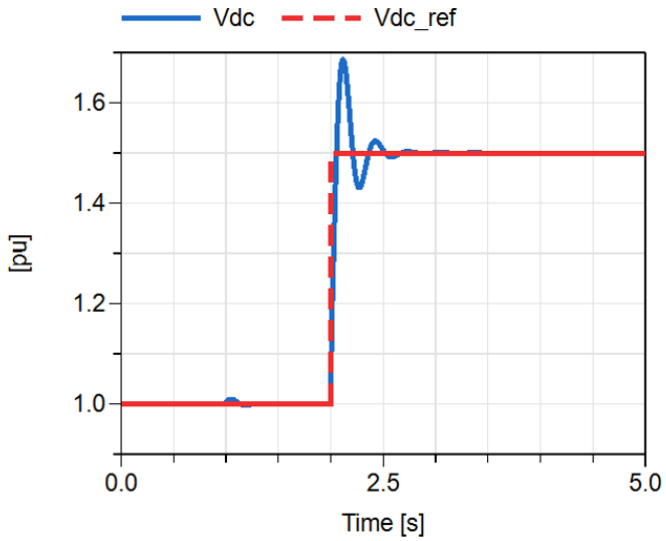
Qac response.

- At t = 1.5 s, *Pac_ref* steps from 0.2 to 0.3 pu (200 to 300 MW on a 1000 MVA base)
- *Active Power, Pac* reaches its new reference within ≈ 200 ms.
- *Reactive Power, Qac* stays at its 0.01 pu reference, so the two power channels are regulated independently.

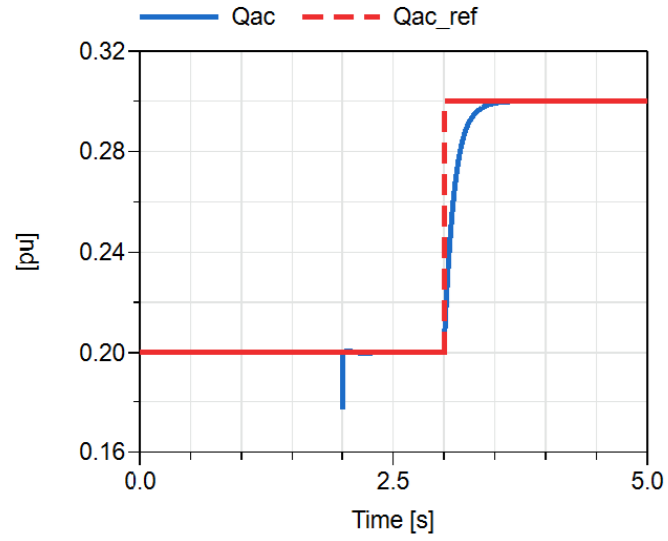
Examples: DC Voltage Mode Test



DCvoltageModeTest model



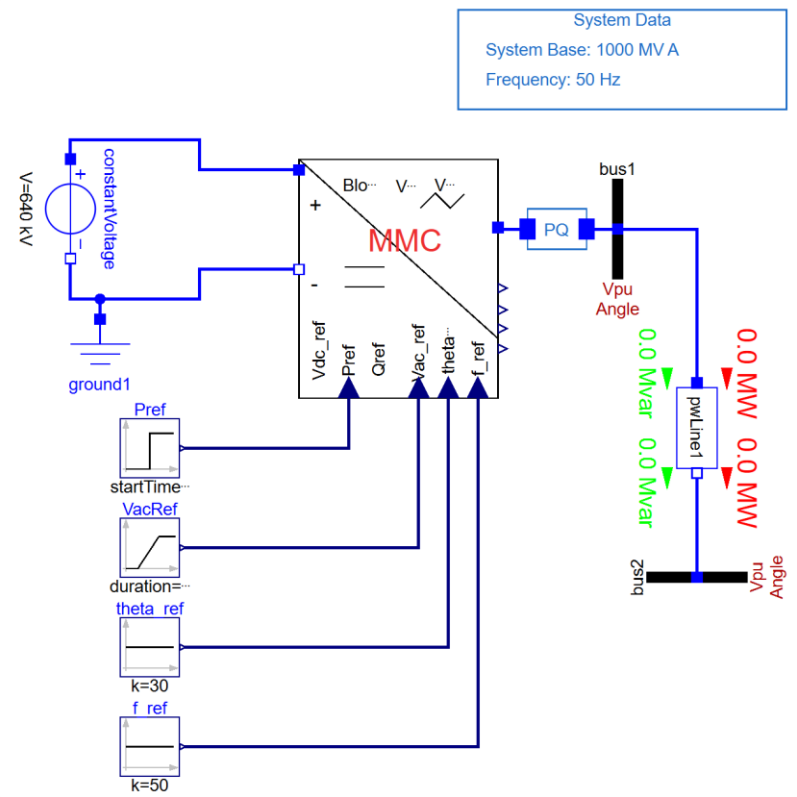
Vdc response;



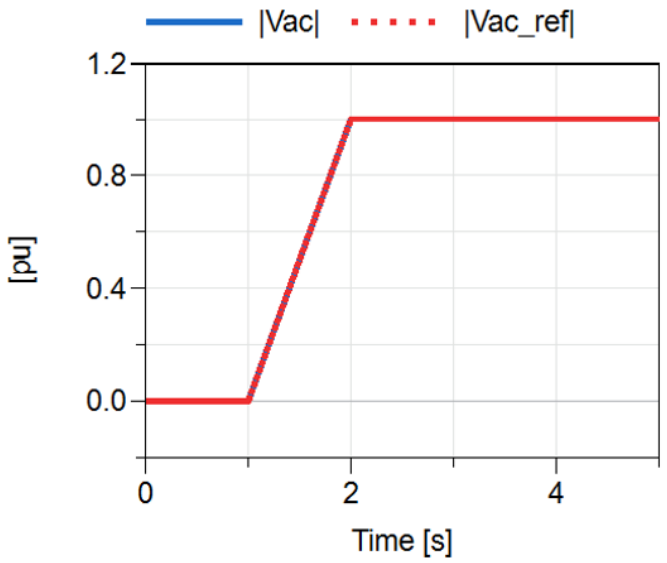
Qac response.

- Vdc_ref is stepped from 1.0 pu to 1.5 pu, and at t = 3 s, the reactive-power reference Qac_ref is stepped from 0.2 pu to 0.3 pu.
- The three events are separated in time so that the rejection of disturbance and reference tracking can be independently assessed.
- **Disturbance rejection:** The current disturbance at t =1 s produces only a small excursion in Vdc, of the order of 0.02 pu, which diminishes within approximately 0.1 s
- **Vdc tracking:** *Vdc_ref* step at t = 2 s is underdamped tracking response, with a peak of about 1.68 pu and a damped oscillation that settles in approximately 0.9 s, without steady-state error.
- **Qac** is unaffected by the DC-side disturbance at t =1 s, and the DC voltage step at t = 2 s causes only a brief dip that recovers quickly

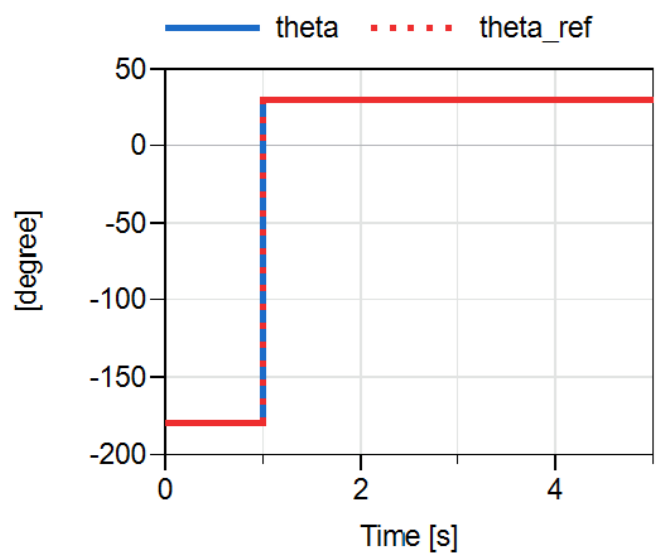
Examples: AC Voltage Mode Test



ACvoltageModeTest model



|Vac| response;



ϑ response.

- The station feeds an AC network at the receiving side; |Vac|, θ and f references are external inputs
- At t = 1 s, |Vac_ref| ramps from 0 to 1.0 pu and θ_ref steps to its specified value.
- **Both the magnitude and the angle of the terminal voltage phasor follow their references**

Conclusions and Future Work

Conclusions

- Open-source, modular Modelica library for phasor-domain AAVM of MMC-HVDC
- P-Q, Vdc-Q and Vac stations plus a configurable master station
- Examples exercise every mode; suited to system-level dynamic studies

Future work

- Quantitative comparison against detailed EMT models
- Create examples for Point-to-point HVDC and multi-terminal DC test systems.
- Integration with larger OpenIPSL AC networks

Library on GitHub: github.com/ALSETLab/MMChvdcLibrary

Thank you! Questions?

Acknowledgement: supported in part by the New York Independent System Operator (NYISO) project "Dynamic Modeling of Voltage Source Converters for Black Start Capability Analysis."

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